

**Amendment To The Claims:**

1           1.       (Currently amended) A content processing unit for protecting interchip  
2 content pathways transporting digital content objects, the content processing unit comprising:  
3           a first chip package, wherein the first chip package comprises:  
4               a first body,  
5               a first plurality of interconnects,  
6               an encryption engine, and  
7               a first key storage register capable of storing a first key, wherein:  
8                   the first key is used by the encryption engine to  
9           produce ciphertext content,  
10               the first key storage register is non-readable from  
11           outside the first body, and  
12               the first key storage register cannot be overwritten  
13           after a programmability period, the programmability period being  
14           a period in which the first key is loaded in the first key storage,  
15           a second chip package, wherein the second chip package comprises:  
16               a second body,  
17               a second plurality of interconnects,  
18               a decryption engine, and  
19               a second key storage register capable of storing a second key,  
20       wherein:  
21               the second key is used by the decryption engine to  
22           produce plaintext content from the ciphertext content, and  
23               the second key storage register is non-readable  
24           from outside the second body, the second key storage register  
25           being writeable while being non-readable;  
26           a content pathway coupling a ~~first~~ subset of the first plurality of interconnects and  
27   a ~~second~~ subset of the second plurality of interconnects, wherein the content pathway transports  
28 the digital content objects as the ciphertext content.

1                   2.       (Currently amended) The content processing unit for protecting interchip  
2 content pathways transporting digital content objects as recited in claim 1, wherein the  
3 programmability period ends when a command is sent to the first plurality of interconnects.

1                   3.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 2, wherein the command  
3 activates a fusible link.

1                   4.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein the programmability  
3 period ends after writing to the first key storage register.

1                   5.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein at least one of the  
3 first and second chip packages comprises a plurality of semiconductor substrates.

1                   6.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein:  
3                   the first chip package further comprises a third key storage register capable of  
4 storing a key encryption key, and  
5                   the first key is protected with the key encryption key outside the first body.

1                   7.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein the second key  
3 storage register is overwritable by manipulating the second plurality.

1                   8.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein:  
3                   the second chip package further comprises a second encryption engine, and  
4                   the second encryption engine uses the second key or another key that is a function  
5 of the second key.

1                   9.       (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 8, further comprising a third

3 chip package comprising a third key that can decrypt ciphertext produced with the second  
4 encryption engine.

1 10. (Original) The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 1, wherein:

3 the content processing unit is part of a larger system comprising a third plurality  
4 of functionally equivalent content processing units, and

5 each of the third plurality uses a different first key to protect their respective  
6 content pathways.

1 11. (Currently amended) A method for protecting interchip content pathways  
2 transporting digital content objects within a content processing unit, the method comprising steps  
3 of:

4 loading a first key into a first key storage register in a first chip package, wherein  
5 the first key in the first key storage register is non-readable from outside the first chip package;

6 activating a feature of the first chip package that prevents overwriting the first key  
7 in the first key storage register from outside the first chip package, after a period in which the  
8 first key is loaded in the first key storage;

9 encrypting digital content with the first key to produce ciphertext content;

10 coupling the ciphertext content from the first chip package to a content pathway;

11 loading a second key into a second key storage register in a second chip package,  
12 wherein the second key in the second key storage register is non-readable from outside the  
13 second chip package, the second key storage register being writeable while being non-readable;

14 coupling the ciphertext content from the content pathway to a second chip  
15 package; and

16 decrypting the ciphertext content with the second key to reformulate the digital  
17 content.

1 12. (Original) The method for protecting interchip content pathways  
2 transporting digital content objects within the content processing unit as recited in claim 11,  
3 further comprising steps of:

4 loading a key encryption key into a third key storage register in the first chip  
5 package; and  
6 decrypting the first key with the key encryption key, whereby the first key is  
7 protected with the key encryption key outside the first chip package.

1 13. (Original) The method for protecting interchip content pathways  
2 transporting digital content objects within the content processing unit as recited in claim 11,  
3 further comprising a step of overwriting the second key in the second key storage register from  
4 outside the second chip package.

1 14. (Original) The method for protecting interchip content pathways  
2 transporting digital content objects within the content processing unit as recited in claim 11,  
3 further comprising steps of:  
4 encrypting the digital content in the second chip package to produce second  
5 ciphertext content using the second key or another key that is a function of the second key,  
6 coupling the second ciphertext content to a second content pathway.

1 15. (Original) The method for protecting interchip content pathways  
2 transporting digital content objects within the content processing unit as recited in claim 11,  
3 wherein:  
4 the content processing unit is part of a larger system comprising a plurality of  
5 functionally equivalent content processing units, and  
6 each of the plurality uses a different first key to protect their respective content  
7 pathways.

1 16. (Original) A computer system adapted to perform the computer-  
2 implementable method for protecting interchip content pathways transporting digital content  
3 objects within the content processing unit of claim 11.

1 17. (Original) A computer-readable medium having computer-executable  
2 instructions for performing the computer-implementable method for protecting interchip content  
3 pathways transporting digital content objects within the content processing unit of claim 11.

1           18.     (Currently amended) A content processing unit for protecting interchip  
2 content pathways transporting digital content objects, the content processing unit comprising:

3           a first chip package, wherein the first chip package comprises:

4                 a first body,

5                 a first plurality of interconnects,

6                 an encryption engine, and

7                 a first key storage register capable of storing a first key, wherein:

8                         the first key is used by the encryption engine to

9 produce ciphertext content,

10                        the first key storage register is non-readable from

11 the first plurality of interconnects, and

12                        the first key storage register cannot be overwritten

13 after being written once after a period in which the first key is

14 loaded in the first key storage;

15 a second chip package, wherein the second chip package comprises:

16                 a second body,

17                 a second plurality of interconnects,

18                 a decryption engine, and

19                 a second key storage register capable of storing a second key,

20 wherein:

21                        the second key is used by the decryption engine to

22 produce plaintext content from the ciphertext content, and

23                        the second key storage register is non-readable

24 from the second plurality of interconnects, the second key storage

25 register being writeable while being non-readable;

26           a content pathway coupling a ~~first~~ subset of the first plurality of interconnects and  
27 a ~~second~~ subset of the second plurality of interconnects, wherein the content pathway transports  
28 the digital content objects as the ciphertext content.

1           19.     (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 18, wherein:

3           the first key storage register has a third plurality of bits, and  
4           each of the third plurality can only be written once.

1           20.     (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 18, wherein:

3           the first chip package further comprises a third key storage register capable of  
4 storing a key encryption key, and

5           the first key is protected with the key encryption key outside the first body.

1           21.     (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 18, wherein the second key  
3 storage register is overwritable from outside the second chip package.

1           22.     (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 18, wherein:

3           the second chip package further comprises a second encryption engine, and

4           the second encryption engine uses the second key or another key that is a function  
5 of the second key.

1           23.     (Original)     The content processing unit for protecting interchip content  
2 pathways transporting digital content objects as recited in claim 18, wherein:

3           the content processing unit is part of a larger system comprising a third plurality  
4 of functionally equivalent content processing units, and

5           each of the third plurality uses a different first key to protect their respective  
6 content pathways.